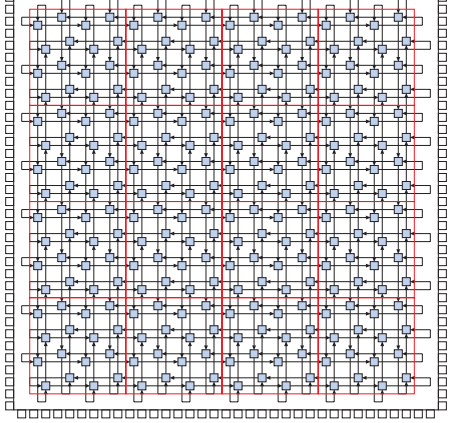
CALL FOR PAPERS

5th Workshop on Highly Parallel Processing on a Chip (HPPC 2011)

August 30, 2011, Bordeaux, France,
http://www.hppc-workshop.org/

to be held in conjunction with

the 17th International European Conference on Parallel and Distributed Computing (Euro-Par)
August 29 - September 2, 2011, Bordeaux, France.



AIMS AND SCOPE

In response to the stagnant growth in single-processor performance single-chip, multi-core parallelism is the most promising solution to the demands for high performance and power efficiency for general purpose, mainstream computing. While both general-purpose architectures with a moderate number of cores and more specialized architectures with a larger number of cores are already on the market, Moore's law predicts future architectures with a significant amount of on-chip parallelism. How the processing power of such architectures can be leveraged for general-purpose computing is a critical issue, as witnessed by the lack of convergence towards a standard model architecture. The design of parallel multi-core architectures that can support manageable parallel programming abstractions to allow the mainstream programmer to take advantage of the processing power furthered by the technological developments is a vital and challenging issue.

The 5th HPPC workshop, co-located with the EuroPar conference, is *the* workshop dedicated to the interface between highly parallel multi-core architectures and programming paradigms, models, and languages that can support parallel algorithms and applications development in an efficient and manageable way. HPPC is intended as a forum for bold, new ideas on architectural organization (general- and special-purpose processors, heterogeneous designs, memory organization, on-chip communication network), parallel programming models, languages, and libraries, multi-core parallel algorithms, and application studies on both existing and envisaged, speculative architectures. Complementary to other multi-core and GPGPU meetings, HPPC stresses programmability and architectural support for more massive levels of parallelism.

Topics of interest include, but are not limited to

° processor core architectures (homogeneous and heterogeneous)
° special purpose processors for general-purpose applications (accelerators, GPUs)
° on-chip memory and cache (or cache-less) organization, and interconnects
° off-chip memory, I/O, and multi-core interconnects
° overall system design (resource allocation and balancing)
° programming models (e.g. PRAM, BSP, data parallel, vector, transactional)
° parallel programming languages and software libraries
° supporting algorithms and implementation techniques (e.g. multi-threading, work-stealing)
° parallel algorithms and applications
° migration of existing codebase
° teaching of parallel computing

for/on highly parallel multi-core systems.

CONTACT INFO

Email: chair@hppc-workshop.org

SUBMISSION

Authors are encouraged to submit original, unpublished research or overviews addressing issues in the design and application of highly parallel multi-core processors as outlined above. Papers should be limited to 10 pages, and typeset in the Springer LNCS style (for details, see www.springer.de/comp/lncs/authors.html). Accepted papers that are presented at the workshop, will be published in revised form in a special Euro-Par Workshop Volume in the Lecture Notes in Computer Science (LNCS) series AFTER the Euro-Par conference. Papers are to be submitted via the Easychair system. Please see the workshop www-page: http://www.hppc-workshop.org

The proceedings of the earlier HPPC workshops have appeared in Springer LNCS Volumes 4854, 5415, and 6043.

IMPORTANT DATES

° Submission of manuscripts: Friday, 10th June, 2011
° Notification of acceptance: Monday, 25th July 2011
° Date of workshop: Tuesday 30th August, 2011
° Deadline for final version (post-proceedings): September, 2011

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