

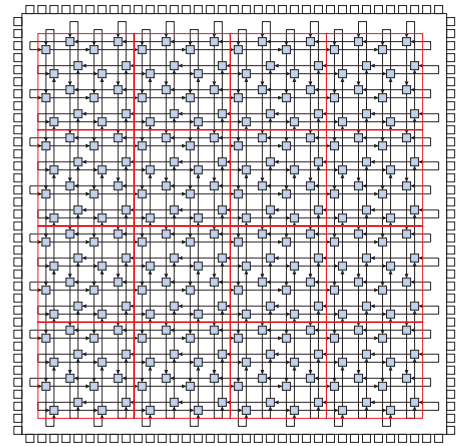
CALL FOR PAPERS

4th Workshop on Highly Parallel Processing on a Chip (HPPC 2010)

August 31, 2010, Ischia - Naples, Italy,
<http://www.hppc-workshop.org/>

to be held in conjunction with

the 16th International European Conference on Parallel and Distributed Computing (Euro-Par)
August 31 - September 3, 2010, Ischia - Naples, Italy.



AIMS AND SCOPE

In response to the stagnant growth in single-processor performance single-chip, multi-core parallelism is envisaged as the solution to the demands for high performance and power efficiency for general purpose, mainstream computing. While new general-purpose architectures with a moderate number of cores are being announced or already on the market, Moore's law predicts architectures with more significant on-chip parallelism, as is already seen for many special purpose processors. How the processing power of such systems can be leveraged for general purpose computing is a critical issue, as witnessed by the lack of convergence towards a standard model architecture. A major challenge for the coming years will therefore be the design of parallel multi-core architectures that can support manageable programming abstractions to allow the mainstream programmer to take advantage of the processing power furthered by the technological developments.

HPPC, the fourth workshop in the series, co-located with the EuroPar conference, is *the* workshop dedicated to the interface between multi-core architectures and programming paradigms, models, and languages that can support parallel algorithms and applications development in an efficient and manageable way. HPPC is a forum for bold, new ideas on architectural organization (general- and special-purpose processors, heterogeneous designs, memory organization, on-chip communication network), parallel programming models, languages, and libraries, multi-core parallel algorithms, and application studies on both existing and envisaged architectures. The workshop will be conducted in an informal atmosphere with room for interaction and discussion between presenters and audience.

Topics of interest include, but are not limited to

- processor core architectures (homogeneous and heterogeneous)
- special purpose processors (accelerators, GPUs)
- on-chip memory and cache (or cache-less) organization, and interconnects
- off-chip memory, I/O, and multi-core interconnects
- overall system design (resource allocation and balancing)
- programming models (e.g. PRAM, BSP, data parallel, vector, transactional)
- parallel programming languages and software libraries
- supporting algorithms and implementation techniques (e.g. multi-threading, work-stealing)
- parallel algorithms and applications
- migration of existing codebase
- teaching of parallel computing

for/on highly parallel multi-core systems.

CONTACT INFO

Email: chair@hppc-workshop.org

SUBMISSION

Authors are encouraged to submit original, unpublished research or overviews addressing issues in the design and application of highly parallel multi-core processors as outlined above. Papers should be limited to 10 pages, and typeset in the Springer LNCS style (for details, see www.springer.de/comp/lncs/authors.html). Accepted papers that are presented at the workshop, will be published in revised form in a special Euro-Par Workshop Volume in the Lecture Notes in Computer Science (LNCS) series AFTER the Euro-Par conference. Please see the workshop [www-page](http://www.hppc-workshop.org): <http://www.hppc-workshop.org>

The proceedings of the earlier HPPC workshops have appeared in Springer LNCS Volumes 4854 and 5415.

IMPORTANT DATES

- Submission of manuscripts: Monday, 14th June, 2010
- Notification of acceptance: Monday, 26th July 2010
- Date of workshop: Tuesday 31st August, 2010
- Deadline for final version (post-proceedings): September, 2010

WORKSHOP ORGANIZERS

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