

# 2008 International Workshop on Multi-Core Computing Systems (MuCoCoS'08)

Barcelona, Spain, March 4 - 7, 2008; in conjunction with CISIS'08

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- **Pierre Michaud**  
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## Context

-The improvement of the processor performance by increasing the clock rate has reached its technological limits. Increasing the number of processor cores rather than clock rate can give better performance and reduce problems like energy consumption, heat dissipation and design complexity. We are witnessing the emergence of multi-core processors in all markets from laptops and game consoles to servers and super-computers.

## Topics of Interest

- The topics of the workshop include but are not limited to:

- multi-core architectures
- interconnection networks
- multi-core embedded systems
- programming languages and models
- algorithms for multi-core computing systems
- applications for multi-core systems
- performance modeling and evaluation of multi-core systems
- design space exploration
- resource usage optimization
- tool-support for multi-core systems
- compilers, runtime and operating systems

## Submission Guidelines

- The papers should be prepared using the [IEEE CS format](http://www.ieee.org/portal/pages/pubs/transactions/stylesheets.html) (<<http://www.ieee.org/portal/pages/pubs/transactions/stylesheets.html>>) and no longer than 6 pages. Submitted papers will be carefully evaluated based on originality, significance to workshop topics, technical soundness, and presentation quality.

- Submission of the paper implies that should the paper be accepted, at least one of the authors will register and present the paper at the workshop. Proceedings of the workshop will be published by [IEEE Computer Society Press](http://www.ieee.org/portal/pages/pubs/transactions/stylesheets.html). The best papers presented at the workshop will be selected for publication in an international journal.

- The papers should be submitted electronically via [CISIS'08 website](http://www.cisis-conference.eu/) <<http://www.cisis-conference.eu/>>

## Important Dates

- Paper submission: CLOSED
- Notification: December 10, 2007
- Registration: December 20, 2007
- Final version of the paper: January 2, 2008
- Workshop: March 4 - 7, 2008

## Keynote Speaker

- **David A. Bader**  
Head of the Sony-Toshiba-IBM center of competence for the Cell BE processor.  
Georgia Institute of Technology, USA  
<<http://www.cc.gatech.edu/~bader/>>