

# Call for Papers

## The 4<sup>th</sup> IEEE International Workshop on Multicore and Multithreaded Architectures and Algorithms (M2A2 2012)

July 10-13, 2012, Madrid, Spain

### General Co-Chairs

Houcine Hassan, Spain  
Julio Sahuquillo, Spain

<http://www.arcos.inf.uc3m.es/ispa2012/CFP-M2A2-12.pdf>

### Steering Committee

Laurence T. Yang, Canada  
Jong Hyuk Park, Korea

In conjunction with

## The 10<sup>th</sup> IEEE International Symposium on Parallel and Distributed Processing with Applications

<http://www.arcos.inf.uc3m.es/ispa2012/>

### Program Committee (TBC)

Hideharu Amano, Japan  
Hamid R. Arabnia, USA  
Luca Benini, Italy  
Luis Gomes, Portugal  
Zonghua Gu, Hong Kong  
Rajiv Gupta, USA  
Houcine Hassan, Spain  
Seongsoo Hong, Korea  
Shih-Hao Hung, Taiwan  
Eugene John, USA  
Seon Wook Kim, Korea  
Jihong Kim, Korea  
Chang-Gun Lee, Korea  
Sebastian Lopez, Spain  
Yoshimasa Nakamura, Japan  
Sabri Pllana, Austria  
Sami Yehia, France  
Yang Xiang, Australia  
Julio Sahuquillo, Spain  
Zili Shao, Hong Kong  
Kenjiro Taura, Japan



Multicore systems are dominating the processor market ranging from embedded to high-performance systems. Early multicore processors just included two or four cores; currently some processors integrate more than ten cores and, as the node shrinks in future technology generations, it is expected that the number of cores will continue increasing in future manufactured systems.

To take advantage of the high number of cores efficient load balancing and scheduling policies or strategies are required. In addition, it remains a challenge to identify and productively program applications for these systems with a resulting substantial performance improvement.

On the other hand, the system designer must trade off performance versus power consumption, which is a major concern in current microprocessors. Therefore current design must focus on new architectures or architectural mechanisms addressing this trade off.

Finally, most real-time embedded applications are requiring high-performance computing and multicore and multithreaded processors are becoming the typical design choice.

The aim of this workshop is to provide a forum for engineers and scientists to address the resulting challenge and to present new ideas, applications, and experience on all aspects of multicore and multithreaded systems.

Authors are invited to submit high quality papers representing their original work in (but not limited to) the following topics targeting multicore multithreaded processors:

- Multicore and multithreaded architectures
- Power-aware multicore architectures and computing
- Embedded multicore real-time systems
- Scheduling and load balancing
- Multicore programming
- Parallel and distributed algorithms

## **Paper Submission and Publication**

Submit original unpublished papers in PDF or Ms-Word formats at the ISPA-2012 submission system: <https://www.easychair.org/account/signin.cgi?conf=ispa2012>, please select Track " Multicore and Multithreaded Architectures and Algorithms". All submitted manuscripts will be reviewed at least by three expert reviewers. Submissions will be judged on originality, technical strength, quality of presentation, and relevance to the workshop scope.

All accepted papers will be included in the ISPA-2012 workshop proceeding published by IEEE Computer Society. The length of the camera-ready manuscripts will be limited to 8 pages in IEEE CS proceedings paper format. Authors of accepted papers, or at least one of them, are requested to register and present their work at the conference, otherwise their papers will not be published.

Distinguished papers accepted and presented in M2A2 2012, after further revisions, could be considered for publication in special issues of SCI indexed international journals.

## **Important Dates**

February 28, 2012: Paper Submission Due

March 15, 2012: Notification of Acceptance/Rejection

April 15, 2012: Camera-Ready Due

July 10-13, 2012: Workshop Takes Place

## **Contact information:**

Houcine Hassan (husein@disca.upv.es)

Julio Sahuquillo (jsahuqui@disca.upv.es)

Department of Computer Engineering.

Universidad Politecnica de Valencia.

Camino de Vera, 14

46022 Valencia, Spain